In The Claims:

1. A method for translating virtual address information in a computer system, comprising:

accessing a first translation lookaside buffer (TLB) by a first memory port and a second memory port;

accessing a second TLB by the first and the second memory ports, and by a third memory port and a fourth memory port;

receiving first virtual address information in the first TLB; and

in parallel with receiving the first virtual address information in the first TLB, receiving the first virtual address information and second virtual address information in the second TLB.

2. The method of claim 1, wherein the first virtual address information consists of integer load information.

3. The method of claim 1, wherein the second virtual address information comprises one or more of integer store data and floating point load and store data and TLB reference and update instructions.

4. The method of claim 1, further comprising:

converting the first virtual address information into TLB hit information; and

providing the TLB hit information to a first cache.

5. The method of claim 1, further comprising:

converting the second virtual address information into physical address information; and

providing the physical address information to a first cache and to a second cache.

6. The method of claim 1, further comprising storing exception and privilege information in the second TLB.

7. A parallel, distributed function translation lookaside buffer (TLB) structure, comprising:

a small TLB having a reduced memory port bandwidth, the small TLB adapted to receive address data consisting of address data associated with integer loads; and

a large TLB having a high memory port bandwidth, the large TLB operable in parallel with the small TLB, the large TLB adapted to receive the address data associated with the integer loads and adapted to receive address data associated with floating point operations and integer store operations.

8. The TLB structure of claim 7, further comprising:

an integer load data cache that receives an output from the small TLB; and

a data cache that receives an output from the large TLB, wherein the small TLB provides TLB hit information based on a virtual address and the integer load data cache stores the TLB hit information, and wherein the large TLB provides physical addresses to the data cache and the data cache holds the physical address.

9. The TLB structure of claim 7, wherein the small TLB is accessed by first memory ports and the large TLB is accessed by the first memory ports and by second memory ports.

10. The TLB structure of claim 7, further comprising a store update and invalidate control coupled to the large TLB and the integer load data cache, the store update and invalidate control providing an update or invalidation signal for cache lines in the integer load data cache.

11. The TLB structure of claim 7, further comprising an exception and privilege information module, wherein the large TLB receives exception and privilege information.

12. A method to reduce latency and thrashing in a computer architecture having a parallel translation lookaside buffer (TLB) structure, the method, comprising:

providing integer load address information to a first TLB using a first bandwidth; and

providing the integer load address information, and other address information, to a second TLB using a second bandwidth larger than the first bandwidth, wherein the integer load address information is provided in parallel to the first and the second TLBs.

13. The method of claim 12, further comprising:

converting the integer load address information into TLB hit information; and

providing the TLB hit information to a first cache.

14. The method of claim 12, further comprising:

converting the integer load address information, and other address information into physical address information; and

providing the physical address information to a first cache and to a second cache.

15. The method of claim 12, further comprising storing exception and privilege information in the second TLB.